

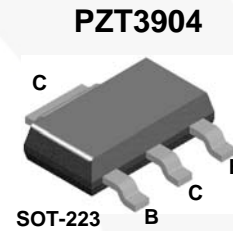
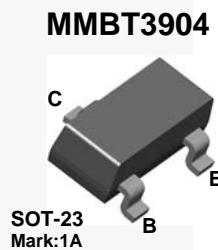
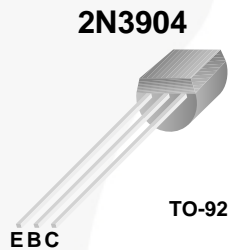


October 2014

## 2N3904 / MMBT3904 / PZT3904 NPN General-Purpose Amplifier

### Description

This device is designed as a general-purpose amplifier and switch. The useful dynamic range extends to 100 mA as a switch and to 100 MHz as an amplifier.



### Ordering Information

Part Number	Marking	Package	Packing Method	Pack Quantity
2N3904BU	2N3904	TO-92 3L	Bulk	10000
2N3904TA	2N3904	TO-92 3L	Ammo	2000
2N3904TAR	2N3904	TO-92 3L	Ammo	2000
2N3904TF	2N3904	TO-92 3L	Tape and Reel	2000
2N3904TFR	2N3904	TO-92 3L	Tape and Reel	2000
MMBT3904	1A	SOT-23 3L	Tape and Reel	3000
PZT3904	3904	SOT-223 4L	Tape and Reel	2500

2N3904 / MMBT3904 / PZT3904 — NPN General-Purpose Amplifier

## Absolute Maximum Ratings<sup>(1), (2)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CEO}$	Collector-Emitter Voltage	40	V
$V_{CBO}$	Collector-Base Voltage	60	V
$V_{EBO}$	Emitter-Base Voltage	6.0	V
$I_C$	Collector Current - Continuous	200	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Notes:

1. These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3904	MMBT3904 <sup>(3)</sup>	PZT3904 <sup>(4)</sup>	
$P_D$	Total Device Dissipation	625	350	1,000	mW
	Derate Above $25^\circ\text{C}$	5.0	2.8	8.0	$\text{mW}/^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	$^\circ\text{C}/\text{W}$

### Notes:

3. Device is mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.
4. Device is mounted on FR-4 PCB 36 mm X 18 mm X 1.5 mm, mounting pad for the collector lead minimum  $6\text{ cm}^2$ .

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0\text{ mA}, I_B = 0$	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10\text{ }\mu\text{A}, I_E = 0$	60		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\text{ }\mu\text{A}, I_C = 0$	6.0		V
$I_{BL}$	Base Cut-Off Current	$V_{CE} = 30\text{ V}, V_{EB} = 3\text{ V}$		50	nA
$I_{CEX}$	Collector Cut-Off Current	$V_{CE} = 30\text{ V}, V_{EB} = 3\text{ V}$		50	nA
<b>ON CHARACTERISTICS<sup>(5)</sup></b>					
$h_{FE}$	DC Current Gain	$I_C = 0.1\text{ mA}, V_{CE} = 1.0\text{ V}$	40		
		$I_C = 1.0\text{ mA}, V_{CE} = 1.0\text{ V}$	70		
		$I_C = 10\text{ mA}, V_{CE} = 1.0\text{ V}$	100	300	
		$I_C = 50\text{ mA}, V_{CE} = 1.0\text{ V}$	60		
		$I_C = 100\text{ mA}, V_{CE} = 1.0\text{ V}$	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$		0.2	V
		$I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$		0.3	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$	0.65	0.85	V
		$I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$		0.95	
<b>SMALL SIGNAL CHARACTERISTICS</b>					
$f_T$	Current Gain - Bandwidth Product	$I_C = 10\text{ mA}, V_{CE} = 20\text{ V},$ $f = 100\text{ MHz}$	300		MHz
$C_{obo}$	Output Capacitance	$V_{CB} = 5.0\text{ V}, I_E = 0,$ $f = 100\text{ kHz}$		4.0	pF
$C_{ibo}$	Input Capacitance	$V_{EB} = 0.5\text{ V}, I_C = 0,$ $f = 100\text{ kHz}$		8.0	pF
NF	Noise Figure	$I_C = 100\text{ }\mu\text{A}, V_{CE} = 5.0\text{ V},$ $R_S = 1.0\text{ k}\Omega,$ $f = 10\text{ Hz to }15.7\text{ kHz}$		5.0	dB
<b>SWITCHING CHARACTERISTICS</b>					
$t_d$	Delay Time	$V_{CC} = 3.0\text{ V}, V_{BE} = 0.5\text{ V}$		35	ns
$t_r$	Rise Time	$I_C = 10\text{ mA}, I_{B1} = 1.0\text{ mA}$		35	ns
$t_s$	Storage Time	$V_{CC} = 3.0\text{ V}, I_C = 10\text{ mA},$		200	ns
$t_f$	Fall Time	$I_{B1} = I_{B2} = 1.0\text{ mA}$		50	ns

**Note:**

5. Pulse test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2.0\%$ .

## Typical Performance Characteristics

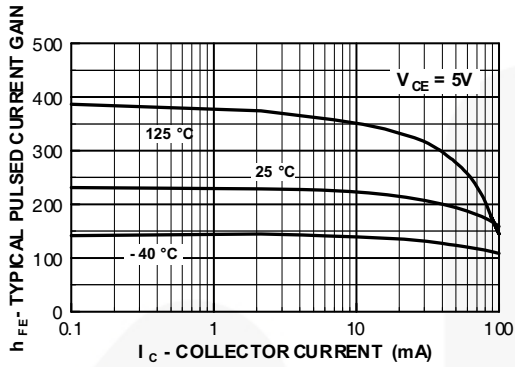


Figure 1. Typical Pulsed Current Gain vs. Collector Current

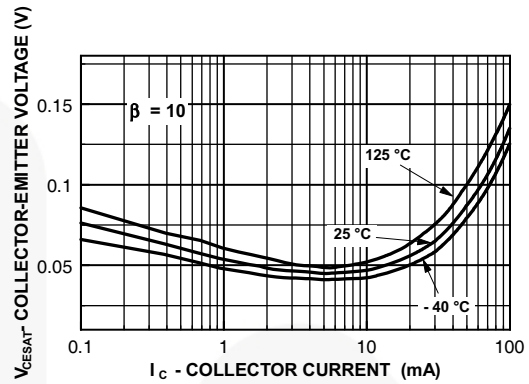


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

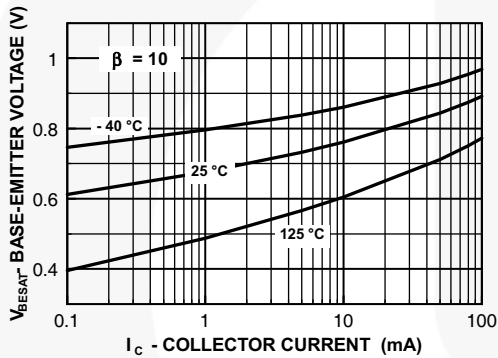


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

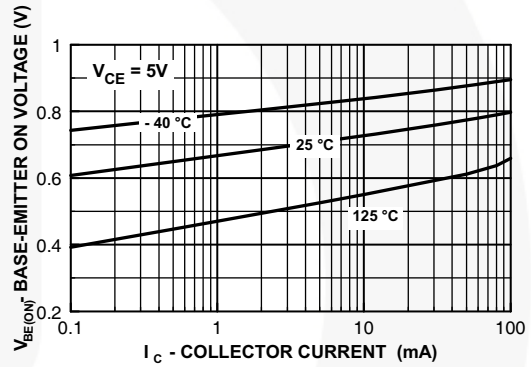


Figure 4. Base-Emitter On Voltage vs. Collector Current

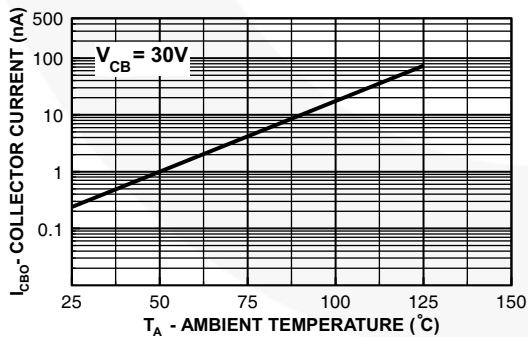


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

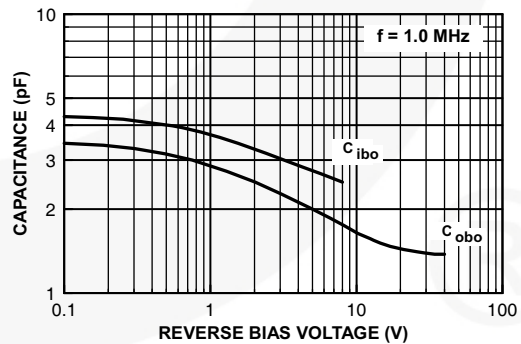
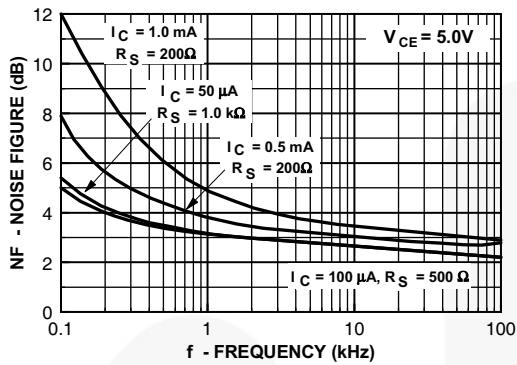
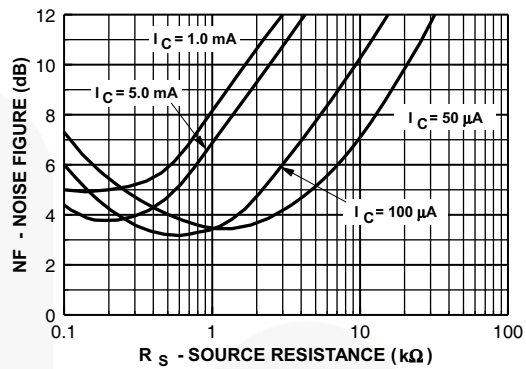


Figure 6. Capacitance vs. Reverse Bias Voltage

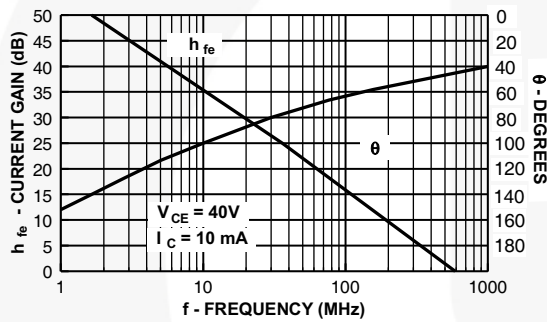
**Typical Performance Characteristics (Continued)**



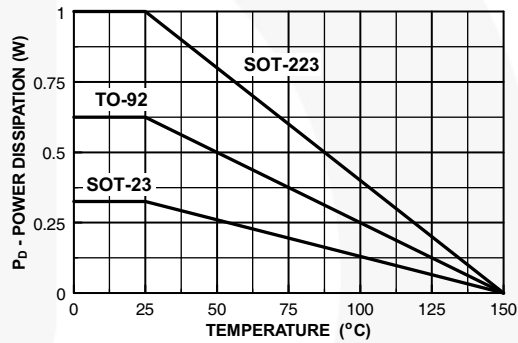
**Figure 7. Noise Figure vs. Frequency**



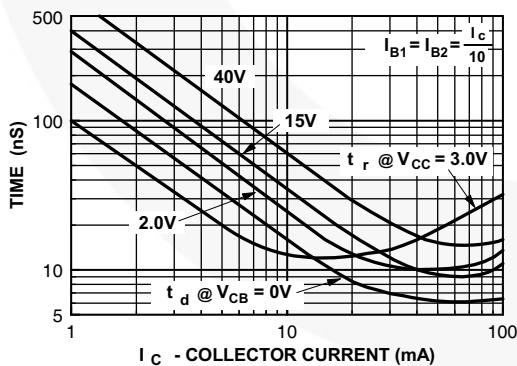
**Figure 8. Noise Figure vs. Source Resistance**



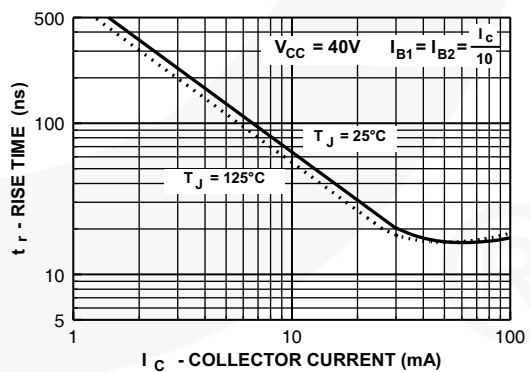
**Figure 9. Current Gain and Phase Angle vs. Frequency**



**Figure 10. Power Dissipation vs. Ambient Temperature**



**Figure 11. Turn-On Time vs. Collector Current**



**Figure 12. Rise Time vs. Collector Current**

Typical Performance Characteristics (Continued)

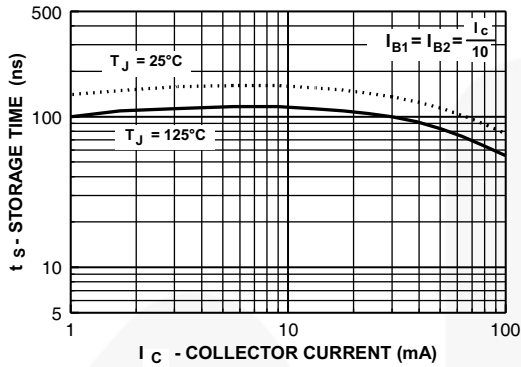


Figure 13. Storage Time vs. Collector Current

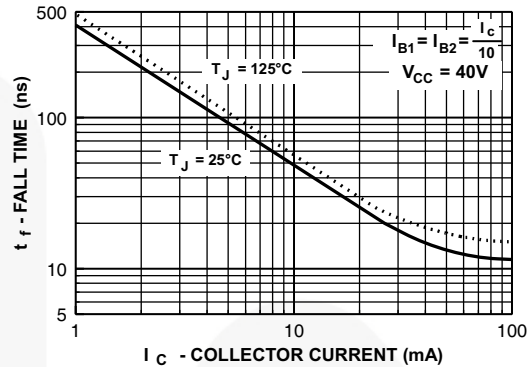


Figure 14. Fall Time vs. Collector Current

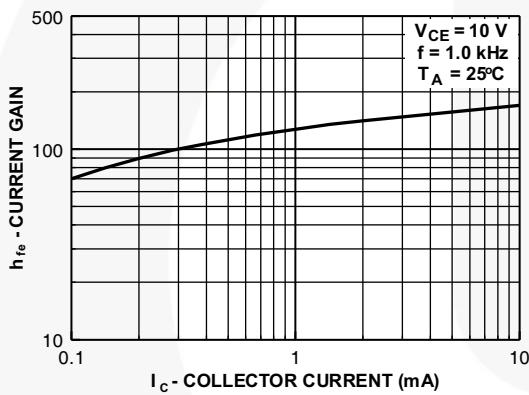


Figure 15. Current Gain

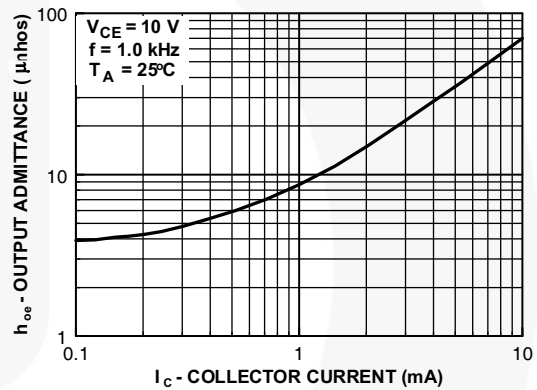


Figure 16. Output Admittance

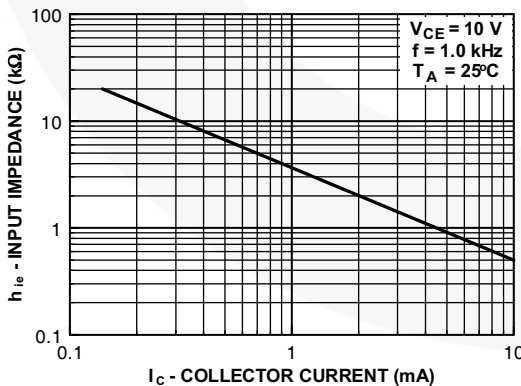


Figure 17. Input Impedance

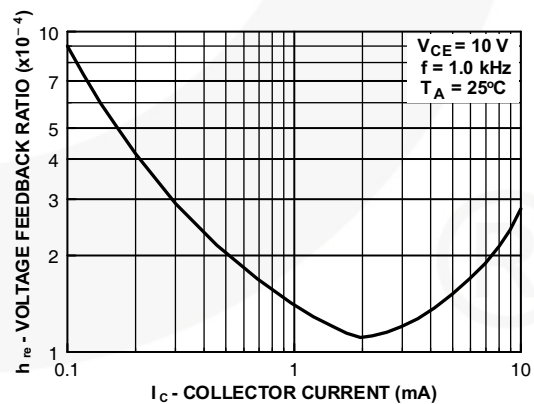


Figure 18. Voltage Feedback Ratio

Test Circuits

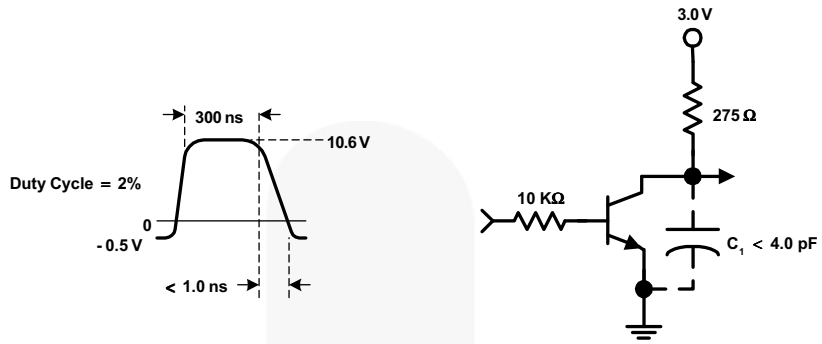


Figure 19. Delay and Rise Time Equivalent Test Circuit

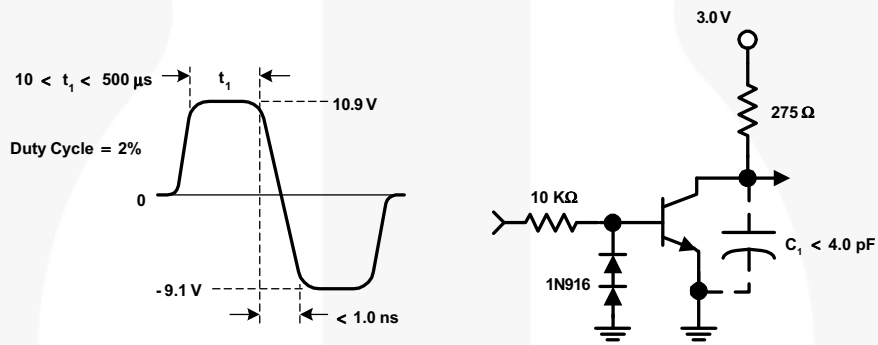
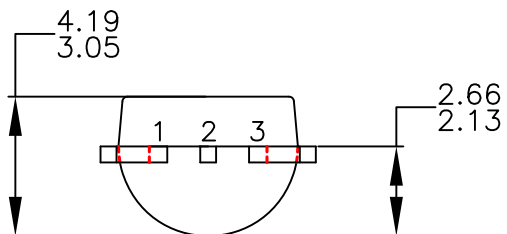
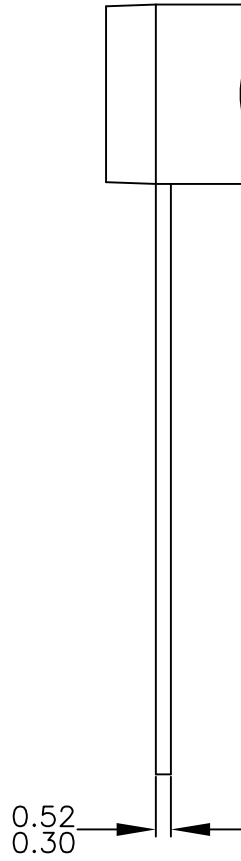
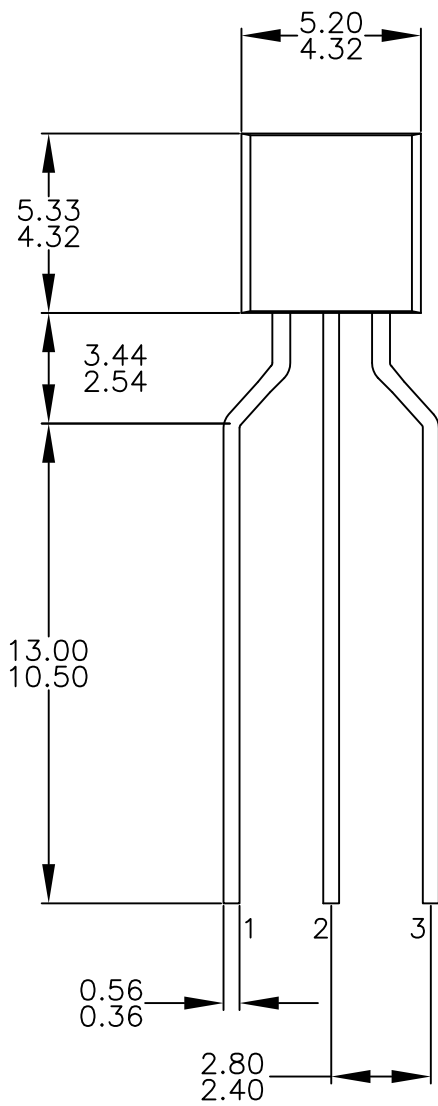


Figure 20. Storage and Fall Time Equivalent Test Circuit



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

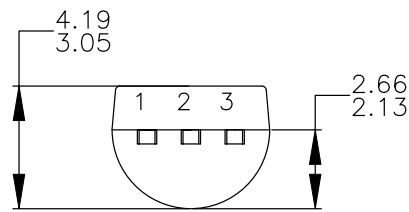
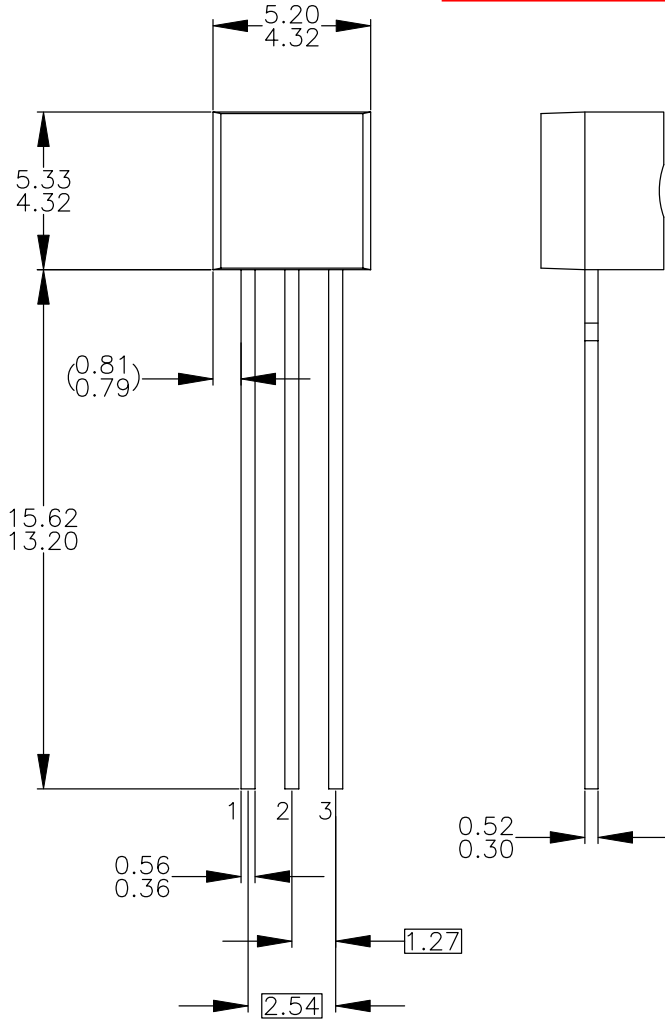


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**APPROVED**  
July-14-2008

**REVISIONS**

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH(MM) TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14-1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32- 4.70 TO 4.32-4.83; CHG PKG HEIGHT DIM FR 4.32-4.70 TO 4.32-4.78; CHG LD THICK DIM FR 0.30- 0.48 TO 0.30-0.52; DAMBAR-PKG DIM FR 1.27-1.65 TO 0.90-1.65; LD LGH DIM FR 14.47-15.64 TO 14.47-15.62; PKG DIM: 1.02-1.52 TO 0.92-1.52, 3.81-4.45 TO 3.40-4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C. MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR <del>13.81</del> TO <del>13.80</del> ; CHG MOLD BODY HT FR <del>4.32</del> TO <del>4.32</del> ; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO (0.81); CHG MOLD BODY WIDTH FR <del>4.32</del> TO <del>4.32</del> ; ADD PKG THICKNESS DIM "E"; CHG "S" DIM FR <del>2.13</del> TO <del>2.13</del> ; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M-1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP



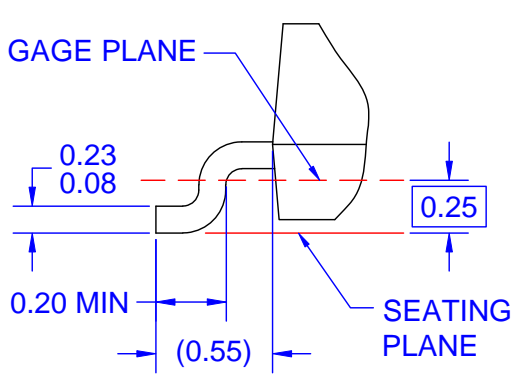
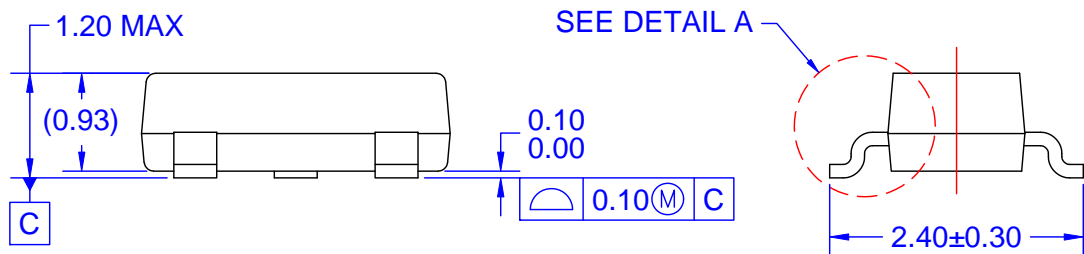
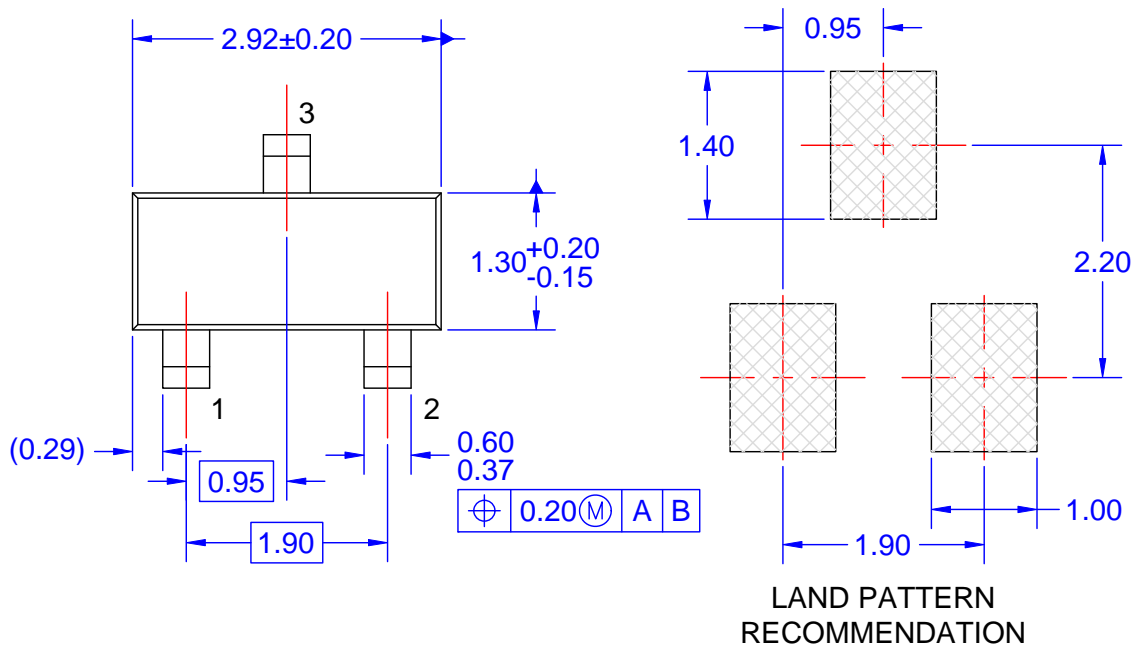
- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DRAWING CONFORMS TO ASME Y14.5M-1994.
  - D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:  
P - BIPOLAR      E - EMITTER      D - DRAIN  
F - JFET          B - BASE              S - SOURCE  
M - DMOS        C - COLLECTOR      G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

APPROVALS	DATE	<b>FAIRCHILD</b> SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	03APR2008	
CHECKED: L. GALERA		
APPROVED: M.R. GESTOLE		
G.S. BAJE		3LD, TO-92, MOLDED STD STRAIGHT LD (NO EOL CODE)
PROJECTION 		SCALE: 1:1
INCH (MM)		SIZE: N/A
		DRAWING NUMBER: MKT-ZA03D
		REV: 3
		FORMERLY: N/A
		SHEET: 1 OF 1



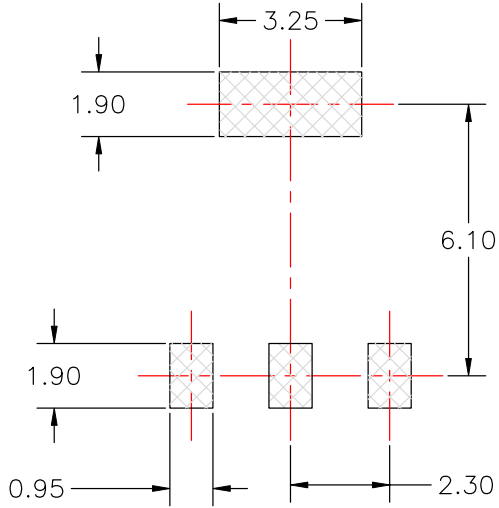
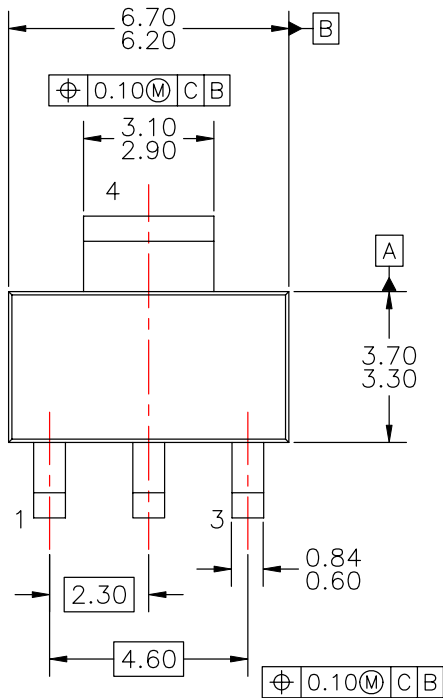
**DETAIL A**  
 SCALE: 2X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
  - E) DRAWING FILE NAME: MA03DREV10

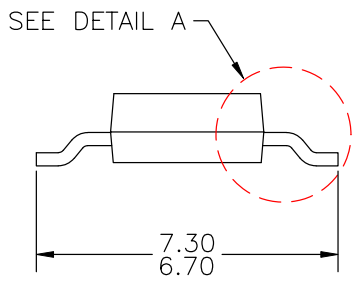
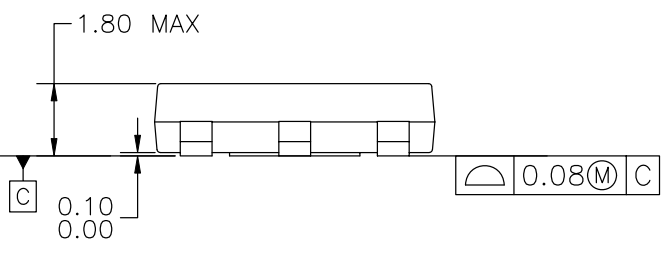
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**APPROVED**  
July-14-2008

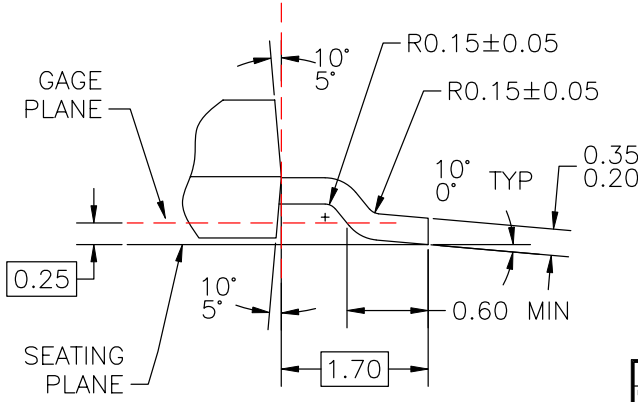
REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 <del>±0.03</del> TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.80 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 <del>±0.03</del> TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 <del>±0.33</del> TO 3.30; CHG BODY LN FR 6.53 <del>±0.33</del> TO 6.30; CHG TOTAL PKG WID FR 6.94 <del>±0.33</del> TO 7.30; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
  - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - C) ALL DIMENSIONS ARE IN MILLIMETERS.
  - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
  - E) LANDPATTERN NAME: SOT230P700X180-4BN
  - F) DRAWING FILENAME: MKT-MA04AREV2



DETAIL A  
SCALE: 2:1

APPROVALS	DATE	<b>FAIRCHILD</b> SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	26FEB2008	
CHECKED: L.Z. STA CRUZ		
APPROVED: M.R. GESTOLE		
G.S. BAJE		<b>MOLDED PACKAGE</b> <b>SOT-223, 4 LEAD</b>
PROJECTION 	SCALE 1:1	SIZE A3
INCH (MM)	DRAWING NUMBER MKT-MA04A	REV 2
	FORMERLY: N/A	SHEET : 1 OF 1



### TRADEMARKS

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AccuPower™	F-PFS™	OPTOPLANAR®	
Awinda®	FRFET®		TinyBoost®
AX-CAP®*	Global Power Resource <sup>SM</sup>	PowerTrench®	TinyBuck®
BitSiC™	GreenBridge™	PowerXS™	TinyCalc™
Build it Now™	Green FPS™	Programmable Active Droop™	TinyLogic®
CorePLUS™	Green FPS™ e-Series™	QFET®	TINYOPTO™
CorePOWER™	Gmax™	QS™	TinyPower™
CROSSVOLT™	GTO™	Quiet Series™	TinyPWM™
CTL™	IntelliMAX™	RapidConfigure™	TinyWire™
Current Transfer Logic™	ISOPLANAR™		TranSiC™
DEUXPEED®	Making Small Speakers Sound Louder and Better™	Saving our world, 1mW/W/kW at a time™	TriFault Detect™
Dual Cool™	MegaBuck™	SignalWise™	TRUECURRENT®*
EcoSPARK®	MICROCOUPLER™	SmartMax™	μSerDes™
EfficientMax™	MicroFET™	SMART START™	
ESBC™	MicroPak™	Solutions for Your Success™	UHC®
	MicroPak2™	SPM®	Ultra FRFET™
Fairchild®	MillerDrive™	STEALTH™	UniFET™
Fairchild Semiconductor®	MotionMax™	SuperFET®	VCX™
FACT Quiet Series™	MotionGrid®	SuperSOT™-3	VisualMax™
FACT®	MTi®	SuperSOT™-6	VoltagePlus™
FAST®	MTx®	SuperSOT™-8	XS™
FastvCore™	MVN®	SupreMOS®	Xsens™
FETBench™	mWSaver®	SyncFET™	仙童™
FPS™	OptoHiT™	Sync-Lock™	
	OPTOLOGIC®		

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### PRODUCT STATUS DEFINITIONS

#### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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